REMARKS

Claims 1-15 and 38-47 are currently pending in this application. Claims 16-27 are withdrawn. Claims 28-37 were previously canceled. Claims 1 and 38 are amended herein to place the claims in condition for allowance or to place the claims in a better condition for appeal. Applicants respectfully request entry of this amendment and reconsideration in view of the following remarks.

The Applicants thank the Examiner for the courtesy he extended in the telephone interview conducted October 27, 2005. Following the discussion, Applicants have amended the independent claims herein. Applicants have made a diligent effort to place the claims in condition for allowance. Allowance is respectfully requested.

Claims 38-47 were rejected in the Office Action under 35 U.S.C. § 102(e) as being anticipated by Hamamoto. This rejection is hereby respectfully traversed.

The Examiner remarks that the reference discloses each of the limitations of claim 38 and refers to Figures 30 and 31 in the Hamamoto reference.

Applicants have reviewed the reference carefully and have considered the Examiner's remarks. The Hamamoto reference depicts, in Figures 31 and 32 for example, a structure with capacitors for a DRAM formed in a trench, and an access transistor formed laterally on a substrate adjacent the DRAM, the access transistor having a gate contact structure formed on the substrate, with a drain conductive region adjacent one side of the gate contact. A source conductive region is formed adjacent the opposing side of the gate contact and is coupled by conductive material to a plate of the capacitor. A bitline contact is made to the conductive drain region, this material does not contact the source conductive region. Interlevel dielectric insulates the capacitor and source regions from the bitline contact.

The Examiner remarked that Hamamoto discloses each of the elements of claim 38.

Claim 38 is amended herein and now recites:

> A method of forming a semiconductor device, the method comprising:
> forming a plurality of structures over a semiconductor body each structure having sides and a top and extending from a surface of the semiconductor body;
> forming an insulating material between ones of the structures;
> applying a line mask over the semiconductor body, the line mask exposing at least one of the structures and regions of the insulating material adjacent opposing side edges of the at least one of the structures;
> removing the insulating material that is exposed by the line mask to create at least two recesses, the at least two recesses being adjacent the sides of and separated by the at least one of the structures that was exposed by the line mask, each of the recesses exposing a conductive region adjacent the sides of the at least one structure;
> forming a conductive material within the at least two recesses and overlying the at least one structure and disposed adjacent the sides and top of the at least one structure, the conductive material electrically connecting the conductive regions exposed by the at least two recesses; and
> forming a layer of material over the conductive material, such that the conductive material electrically connects the conductive regions at a point in time when the layer of material is formed.

Applicants believe that the reference does not show, teach or suggest the recited methods of claim 38. In particular, the reference does not show, teach or suggest:

> applying a line mask over the semiconductor body, the line mask exposing at least one of the structures and regions of the insulating material adjacent opposing side edges of the at least one of the structures;
> removing the insulating material that is exposed by the line mask to create at least two recesses, the at least two recesses being adjacent the sides of and separated by the at least one of the structures that was exposed by the line mask, each of the recesses exposing a conductive region adjacent the sides of the at least one structure;
> forming a conductive material within the at least two recesses and overlying the at least one structure and disposed adjacent the sides and top of the at least one structure, the conductive material electrically connecting the conductive regions exposed by the at least two recesses; and
> forming a layer of material over the conductive material, such that the conductive material electrically connects the conductive regions at a point in time when the layer of material is formed.

With respect to the step of applying a line mask, the Examiner cited the line mask 62 in Hamamoto. In contrast to the recited line mask, however, line mask 62 does not expose the required areas, but in fact covers the "recess" over the drain conductive region of 23 (see Figure 31), so it cannot meet the method steps recited in the claim.

Likewise, the recited step of "removing the insulating material to create at least two recesses...adjacent the sides of and separated by the at least one of the structures" is not shown or suggested in Hamamoto. The insulating interlevel dielectric material remains in place adjacent one of the sides of the structures after the line mask and removal step, and is not removed. In contrast to the recited method steps of Claim 38, there are not two recesses formed adjacent the sides of the at least one structure as required.

Because the two recesses are not formed adjacent the sides of the at least one structure, the conductive material identified by the Examiner (apparently 6 in Figure 32) cannot be formed within the at least two recesses and disposed adjacent the sides and top of the at least one structure as recited in Applicants' claim 38.

Finally, the material 6 appears to be the last layer formed by Hamamoto. Applicants find no teaching or suggestion in the reference to form the layer of material "over the conductive material" as recited in claim 38.

Further, Applicants submit Hamamoto teaches forming a lateral access transistor with a drain region on one side of a structure, and a source region adjacent the opposing side, which in the circuit of Hamamoto could not be electrically connected. Therefore, it is unsurprising that the reference does not show, teach or suggest the methods of Applicants' claim 38, particularly the recited steps of forming a conductive material in recesses adjacent opposing sides of the structure and "... the conductive material electrically connecting the conductive regions exposed

by the recesses;" because to do so would make the functional circuit, the DRAM of Hamamoto, inoperable.

Applicants conclude that the reference relied upon does not anticipate, or obviate, the method steps of claim 38. Accordingly, Applicants believe the claim is allowable, and reconsideration and allowance is requested.

Claims 39-43 and 47 were also rejected. These dependent claims depend, directly or indirectly, on claim 38 and incorporate the novel steps of claim 38. The Examiner remarked in discussing each claim, that the structure formed in Hamamoto discloses all the claim limitations. However, as the parent claim is now believed to be allowable, so the dependent claims, which incorporate those allowable steps, are also believed to be unanticipated and unobvious over the reference. Reconsideration and allowance are therefore respectfully requested.

Claims 1-5, 8, 44 and 45 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hamamoto in view of Sung. This rejection is also hereby respectfully traversed.

Hamamoto provides a lateral access transistor adjacent to and coupled for accessing a trench capacitor formed in a substrate, as described above. Sung provides a nonvolatile structure with a bit line coupled to plugs formed in vias to a conductive region in a substrate. Like Hamamoto, the Sung reference provides a bit line electrically coupled to drain regions which are adjacent one side of a gate contact, the source region adjacent the opposing side is not coupled to the bit line. The Examiner cites Sung as providing the metal layer required by Claim 1, which is not provided by Hamamoto and remarks that the combination discloses the claimed steps.

Claim 1 is amended herein and now recites:

> A method of fabricating a semiconductor device, comprising:
> patterning a mask on a surface of a semiconductor wafer to expose portions of the
> semiconductor wafer while covering other portions of the semiconductor wafer;
> forming a plurality of recesses between gate contacts disposed in a first region of the semiconductor wafer; the gate contacts having insulating sidewalls and being covered with an insulator, the recesses being formed on opposite sides of and adjacent the insulating sidewalls of the gate contacts;
> depositing a conductive material to fill the recesses and to cover the gate contacts such that a continuous conductive layer of the conductive material fills a first recess adjacent one side of at least one gate contact, extends over the top of the at least one gate contact, and fills the second recess adjacent an opposing side of the at least one gate contact; and
> depositing a metal layer, wherein the metal layer contacts at least a portion of the continuous conductive layer and is in electrical contact with the continuous conductive layer filling the recesses.

Applicants have examined the references and considered the Examiners remarks. The Hamamoto reference does not show, or suggest, the recited method steps of claim 1 and in particular does not show, teach or suggest:

> depositing a conductive material to fill the recesses and to cover the gate contacts such that a continuous conductive layer of the conductive material fills a first recess adjacent one side of at least one gate contact, extends over the top of the at least one gate contact, and fills the second recess adjacent an opposing side of the at least one gate contact;...

As argued above with respect to claim 38, Hamamoto provides a lateral transistor with a drain region adjacent one side of a gate contact structure and a source region adjacent the opposing side of the gate contact structure. The reference does not provide a first recess adjacent one side of a gate contact and a second recess adjacent the opposing side of the gate contact, and a conducive material that fills the first recess, extends over the gate contact and fills the second recess as in Applicants' claimed method. This is unsurprising because the regions adjacent the gate contact in Hamamoto must not be connected if the DRAM circuit is to function.

The Examiner then adds the Sung reference to provide the missing element of "depositing a metal layer..." However, the combination suggested by the Examiner still does not disclose the method steps of claim 1, because the Sung reference also provides structures on a substrate (floating gate devices) with drain regions adjacent one side of the gate contacts and source regions adjacent the opposing sides, the metal layer connects the drain regions of differing gate contacts together, but does not connect the recess regions on either side of a gate contact. As discussed above with respect to Hamamoto, the circuit of Sung also requires that the drains and sources be isolated from each other, and not connected together.

Applicants conclude that the steps of claim 1 are not obviated by the references whether taken singly or in combination, and that the addition of Sung cannot cure the deficiencies of the Hamamoto reference in failing to show or suggest the required method steps. Claim 1 is therefore believed to be allowable over the rejection. Accordingly, reconsideration and allowance of claim 1 is requested.

Claims 2-5 and 8 depend from and add additional steps to the method of claim 1, while incorporating the allowable steps of the parent claim. As claim 1 is now believed to be allowable, these dependent claims are also therefore allowable over the rejection. Reconsideration and allowance are requested.

Similarly, claims 44 and 45 depend from claim 38 and add the additional step of providing a metal layer (44) and a refractory metal layer (45) to the parent claim. As the parent claim is believed to be allowable over Hamamoto, as discussed above, and as Sung does not provide the elements missing from Hamamoto, these dependent claims incorporate allowable steps over the references and are therefore also believed to be allowable. Reconsideration and allowance are requested.

Claims 9 and 46 were rejected under 35 U.S.C. § 103 as being unpatentable over Hamamoto and Sung and further in view of Nitayama et al. This rejection is also hereby respectfully traversed.

The Examiner remarks that Hamamoto and Sung disclose all of the claimed limitations of claims 8 and 45, however claims 9 and 46 require the refractory metal to be tungsten, which is admittedly not disclosed by the combination. Nitayama is then added to the combination to provide the tungsten.

While Nitayama may disclose tungsten, the combination of references taken together as suggested by the Examiner, or singly, does not obviate the parent claims, which as argued above, recite allowable steps not disclosed in the references. Accordingly, these dependent claims are also allowable over the rejection, and reconsideration and allowance are requested.

Claims 10-11 and 14 were rejected under 35 U.S.C § 103 as being unpatentable over Hamamoto and Sung and further in view of Parekh. This rejection is also hereby respectfully traversed.

Claim 10 depends from claim 1 and adds the limitation that the conductive material is silicon. Claim 11 depends from claim 10 and adds the limitation that the silicon is a polysilicon. Claim 14 depends from claim 10 and adds the limitation that the silicon is a doped silicon.

The Examiner remarked that Parekh et al. discloses forming a doped polysilicon conductive layer in contact holes to form a contact plug. The Examiner further remarks again that the combination of Hamamoto and Sung provide the elements of claim 1 and concludes that the dependent claims are therefore obviated.

Applicants reply that as argued above, claim 1 recites steps not disclosed in the Hamamoto and Sung references and the combination. Parekh also discloses source and drain

regions adjacent gate structures, as does Hamamoto and Sung, and thus also fails to disclose the conductive material filling recesses as recited in claim 1, as argued above with respect to Hamamoto and Sung. As these dependent claims therefore recite elements not shown or suggested in any of the references or the combination suggested by the Examiner, Applicants conclude that these dependent claims are also allowable over the rejection. Accordingly, reconsideration and allowance are requested.

Claims 12 and 13 were likewise rejected under 35 U.S.C. § 103 as being unpatentable over Hamamoto, Sung, Parekh and further in view of Taniguchi. This rejection is also respectfully traversed.

Claims 12 and 13 add limitations on the method of claim 10, claim 12 adds that the silicon of claim 10 be an amorphous silicon, and claim 13 adds that the amorphous silicon be annealed. The Examiner remarked that the combination of Hamamoto, Sung and Parekh discloses the limitations of claim 10, and that the Taniguchi reference then discloses the missing elements of using amorphous and annealed amorphous silicon as conductive contact plugs.

Applicants reply that as argued above, with respect to claim 10, the combination of Taniguchi with Sung and Hamamoto fails to disclose the elements of claims 12 and 13 incorporated from claim 1, and that therefore these dependent method claims are also allowable over the references taken singly and in combination. Reconsideration and allowance are therefore requested.

Similarly, claims 6 and 7 were rejected under 35 U.S.C. § 103, as being unpatentable over Hamamoto and Sung and further in view of the Silicon Processing textbook by Wolf et al. This rejection is also hereby respectfully traversed.

Claim 6 depends from claim 5 and adds a limitation that the oxide be formed from a TEOS precursor. Claim 7 further limits claim 6 to at least a 1000Å thick oxide.

The Examiner remarked that the combination of Hamamoto and Sung disclose the limitations of claim 5, including the oxide, but fail to disclose the TEOS or the recited thickness. Wolf is then added to provide the missing elements.

Applicants respond that the parent claims, claims 1 and 5, recite allowable steps over Hamamoto and Sung as argued above. Claims 6 and 7 therefore recite additional method steps on an allowable claim, and as the combination of references does not show or suggest the allowable steps, these dependent claims are also allowable over the rejection. Accordingly, reconsideration and allowance are requested.

Applicants believe that the amendments and arguments herein place this application in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mark E. Courtney, Applicants' attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

11/9/05
Date

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